REMARKS

Claims 1-22 and 24-27 are currently pending in the subject application, and are presently under consideration. Claims 1-11, 16-22, and 24-27 are allowed. Claims 12-15 are rejected. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

Rejection of Claims 12-15 Under 35 U.S.C. §102(b)

Claims 12-15 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,151,568 to Allen ("Allen"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 12 recites a clock gater calculator that determines power consumed by at least one clock gater in a circuit design employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit. A clock gater is defined in the Specification (page 4, ll. 3-15) of the Present Application as a circuit which receives a first clock signal and outputs a second clock signal that is a function of the input clock signal, and might perform some function on the clock signal, such as adjusting the pulse width or frequency, so that the output clock signal has different characteristics than the input clock signal. The clock gater is designed to have a low input capacitance, so as not to overload the system clock and have high current drive capabilities to drive clock enabled logic gates. As stated in the Specification of the Present Application, this type of circuit is difficult to simulate and ignored by most analysis tools.

Allen discloses a technique for calculating dynamic power by calculating the capacitance of the component nets, which is also known as the interconnections between the components (col. 13, ll. 61-65). The power calculation includes calculating the capacitance, area, length, and activity factor of the net, with the net including intermodule nets, intraoperator nets, and clock nets (col. 14, ll. 30-34). An intermodule net is a net that connects power modules (col. 14, ll. 34-35). A clock net is defined as a net that drives one or more clock inputs to registers on the chip (col. 14, ll. 38-39). Accordingly, the nets disclosed by Allen are device interconnections. Thus,

a clock net is merely a device connection that on which a clock signal propagates, and is therefore not a clock gater as defined in the Specification of the Present Application.

Allen also discloses that to calculate the length of the wire of the clock nets, the power estimation module must also compute a number of buffer cells that will be added to the semiconductor chip design, which is unknown during the power consumption estimation (col. 15, ll. 5-15). Accordingly, Allen further does not disclose that the buffer cells are clock gaters, such that the buffer cells have low input capacitance and high current drive capabilities. Assuming *arguendo* that the buffers cells could be clock gaters, Allen discloses that the number of buffer cells is unknown during power consumption estimation, and thus power estimation could not be performed on the buffer cells if they are unknown during power consumption estimation. Therefore, Allen does not disclose a clock gater calculator that determines power consumed by at least one clock gater in a circuit design employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit, as recited in claim 12.

In addition, the cited section of Allen appears to disclose matching power modules with components in a power netlist for determining power associated with circuit components. Allen states that "the power estimation module 76 uses the power netlist and the chosen technology implementation, whether from the technology file, the user-defined technology library, the default or interactively chosen by the user to calculate power." (col. 13, ll. 57-61) However, Allen is silent as to how the power characterization is predetermined. Particularly, Allen does not disclose that the components matched in the power netlist have a predetermined characterization that correlates power as a function of output drive load. Allen discloses that, to calculate the dynamic power consumed when driving capacitive loads, the power estimation module calculates the capacitance of component nets (col. 13, ll. 61-63). However, as described above, the component nets are interconnections between components, and not the components themselves. Accordingly, Allen does not teach employing at least one predetermined characterization that correlates power as a function of output drive load for a given clock gater circuit, as recited in claim 12. Accordingly, Allen does not anticipate claim 12. Withdrawal of

the rejection of claim 12, as well as claims 13-15 which depend therefrom, is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 08-2025.

Respectfully submitted,

Date 1-3-05

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